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EXAMINER
UMEZ ERONINI, LYNETTE T

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,480	QUEK ET AL	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. ✓
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19, 21, 23, 24, 26, 28, and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 5-6;

In claim 11, lines 7-8;

In claim 16, lines 7-8;

In claim 21, lines 7-8; and

In claim 26, lines 7-8, "depositing a second inorganic dielectric layer overlying said first dielectric layer" is indefinite because it is unclear whether the claim requires two (a first and a second) organic dielectric layers that overlie a dielectric layer.

In claim 6, lines 7-8, "depositing a second inorganic dielectric layer overlying said insulating layer" is indefinite because it is unclear whether the claim requires two (a first and a second) inorganic dielectric layers, which overlie an insulation layer.

In claim 3, lines 2-3;

In claim 8, lines 2-3;

In claim 13, lines 2-3;

In claim 19, lines 2-3;

In claim 24, lines 2-3; and

In claim 29, lines 2-3; "organic dielectric layer comprises one of the group containing: polyimides, . . ." is indefinite because of improper use of Markush language. It is suggested the claim be rewritten, "organic dielectric layer is selected from one of the groups consisting of polyimides, . . . and polymers."

In claim 4, lines 2-3,

In claim 9, lines 2-3;

In claim 14, lines 2-3;

In claim 18, lines 2-3;

In claim 23, lines 2-3; and

In claim 28, lines 2-3, "inorganic dielectric layer comprises one of the group containing: CORAL . . ." is indefinite for improper use of Markush language. It is suggested the claim be rewritten, "inorganic dielectric layer is selected from one of the groups consisting of CORAL, . . . and HSQ."

3. Claims 3, 4, 8, 9, 13, 14, 18, 19, 23, 24, 28, and 29 contain the trademark/trade name CORAL, BLACK DIAMOND, FSG, Z3MS, XLK, HOSP, SILK, FLARE, BCB, and MSQ. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods

themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe inorganic- and organic- dielectric materials that have low dielectric constants and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, and 5 and 16, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Huang et al. (US 5,635,423) and Kuo et al. (US 5,869,219).

As pertaining to the said claims, Chow teaches a method for producing coplanar multi-level metal/insulator films on a substrate in which conductive lines as well as stud via metal contacts are simultaneously formed (column 1, lines 10-16), which reads on, forming dual damascene openings in the fabrication of an integrated circuit device. The method comprises:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure **2**);

depositing a quartz insulation layer **5** (first inorganic dielectric) over substrate **2** (column 3, lines 15-16) and "although the preferred embodiment also makes use of

sputtered quartz or composite Si_3N_4/SiO_2 for insulation layers **5** and **8**, other insulation materials, such as spin-on polyimides are also suitable," reads on depositing a first organic dielectric layer overlying said insulating layer;

depositing a second insulation **8** of quartz or a composite Si_3N_4/SiO_2 layer over the structure as shown in **FIG. 2** (column 3, lines 24-27) and " (column 4, lines 24-27) reads on depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching channels (trench) and via holes into the second and first insulation layer (column 2, lines 42-43) reads on,

thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

Chow differs in failing to teach etching a via pattern into the second dielectric layer, **in claims 1 and 16**.

Huang (5635423) teaches forming a via in a second insulative (dielectric) layer (column 6, lines 19-23).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a via in a second dielectric layer as taught by Huang for the purpose of improving the via profile by providing a minimal interwiring spacing as required by high density design rule (Huang, column 5, lines 19-21).

Chow in view of Huang differs in failing to teach using patterned second dielectric layer as a mask, **in claims 1 and 16**.

Kuo teaches polyimide films in semiconductor processing are interlevel dielectrics and protective buffer coats and using polyimide that is made of photosensitive to be used as a mask (column 2, lines 43-48), which reads on using a patterned dielectric layer.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Huang by using polyimide as a mask as taught by Kuo for the purpose of being easily deposited (Kuo, column 2, lines 38-39).

6. Claims 2 and 17 are ejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Huang ('423) and Kuo ('219) as applied to claims 1 and 16 respectively, above, and further in view of Joshi et al. (US 5,955,781).

Chow in view of Huang and Kuo differs in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact semiconductor device structures.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure (column 7, lines 51-63).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Huang and Kuo by forming the

semiconductor device structures as taught by Joshi for the purpose of providing electrical isolation of semiconductor devices while reducing detrimental thermal effects due to electronic activity (Joshi, column 4, lines 21-30).

7. Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow ('648) in view of Huang ('423) and Kuo ('219) as applied to claims 1 and 16 respectively above, and further in view of Wang et al. (US 6,020,269).

Chow in view of Huang and Kuo differs in failing to teach first inorganic dielectric layer comprises one of the following: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen doped FSG, Z3MS, XLX, and HSQ.

Wang teaches, "An oxide layer **16** is formed over the metal layer 12. Although typically silicon dioxide, oxide layer **16** may include any suitable dielectric oxide material or materials, including silicon dioxide, fluorine doped silicon glass (FSG), tetraethylorthosilicate (TEOS), phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), any suitable spin-on glass, or low k polymer materials (column 4, lines 16-22).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Huang and Kuo by replacing quartz (silicon dioxide) with FSG as taught Wang because both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

8. Claims 6, 9, 10, 21, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow ('648) in view of Huang et al. (US 5,635,423).

Chow teaches a method for producing coplanar multi-level metal/insulator films on a substrate in which conductive lines as well as stud via metal contacts are simultaneously formed (column 1, lines 10-16), which reads on, forming dual damascene openings in the fabrication of an integrated circuit device. The method comprises:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure **2**);

depositing a quartz insulation layer **5** (first inorganic dielectric) over substrate **2** (column 3, lines 15-16) and "although the preferred embodiment also makes use of sputtered quartz or composite Si_3N_4/SiO_2 for insulation layers **5** and **8**, other insulation materials, such as spin-on polyimides are also suitable," reads on depositing a first organic dielectric layer overlying said insulating layer;

depositing a second insulation **8** of quartz or a composite Si_3N_4/SiO_2 layer over the structure as shown in **FIG. 2** (column 3, lines 24-27) and " (column 4, lines 24-27) reads on depositing a second inorganic dielectric layer overlying said first dielectric layer;

etching channels (trench) and via holes into the second and first insulation layer (column 2, lines 42-43) reads on,

thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

Chow differs only in failing the teach thereafter etching a via pattern through said second inorganic dielectric layer and first organic dielectric layer to complete said forming of said dual damascene opening in the fabrication of said integrate circuit device, **in claims 6 and 21**.

Huang teaches, "As shown in FIG. 5(b), after removing the first photoresist mask 55, a second photoresist mask 56 is formed on second insulative layer 54, a trench is formed in second insulative layer 54 to include the first opening by a second etching process while extending the first opening as shown in phantom lines. As shown in FIG. 5(c), the trench is formed in second insulative layer 54 while simultaneously extending the first opening through etch stop layer 53 and first insulative layer 52. The dual damascene metallization technique is then employed to simultaneously fill the via and trench with conductive material to form an interconnection wherein the conductive via provides electrical connection between the conductive wiring and substrate (column 6, 29-36).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by using Huang's method of etching a via pattern through a second dielectric layer and a first dielectric for the purpose of improving the dual damascene process by reducing the number of manipulative steps (Huang, column 3, lines 30-33).

9. Claims 7 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Huang ('423) as applied to claims 6 and 21 respectively, above, and further in view of Joshi et al. (US 5,955,781).

Chow in view of Huang differs only in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact semiconductor device structures.

Joshi teaches a dual damascene structure that comprising forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure (column 7, lines 51-63).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming the semiconductor device structures as taught by Joshi for the purpose of providing electrical isolation of semiconductor devices while reducing detrimental thermal effects due to electronic activity (Joshi, column 4, lines 21-30).

10. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow ('648) and Huang ('423) as applied to claims 6 and 21 respectively above, and further in view of Wang et al. (US 6,020,269).

Chow in view of Huang differs only in failing to teach first inorganic dielectric layer comprises one of the following: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen doped FSG, Z3MS, XLX, and HSQ.

Wang teaches, "An oxide layer **16** is formed over the metal layer 12. Although typically silicon dioxide, oxide layer **16** may include any suitable dielectric oxide material or materials, including silicon dioxide, fluorine doped silicon glass (FSG),

tetraethylorthosilicate (TEOS), phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), any suitable spin-on glass, or low k polymer materials (column 4, lines 16-22).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Huang by replacing quartz (silicon dioxide) with FSG as taught Wang since both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

11. Claims 11, 13, and 15 and 26, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow ('648) in view of Huang ('423).

Chow teaches the same method of forming patterned conductive lines with via connections as in claim 1.

Chow differs only in failing to teach etching a via pattern into said second dielectric layer, **in claims 11 and 26**.

Huang teaches forming a via in a second insulative (dielectric) layer (column 6, lines 19-23).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a via in a second dielectric layer as taught by Huang for the purpose of improving the via profile by providing a minimal interwiring spacing as required by high density design rule (Huang, column 5, lines 19-21).

12. Claims 12 and 27 are ejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Huang ('423) as applied to claims 11 and 26 respectively, above, and further in view of Joshi et al. (US 5,955,781).

Chow in view of Huang differs in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact semiconductor device structures.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure (column 7, lines 51-63).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Huang and Kuo by forming the semiconductor device structures as taught by Joshi for the purpose of providing electrical isolation of semiconductor devices while reducing detrimental thermal effects due to electronic activity (Joshi, column 4, lines 21-30).

13. Claims 14 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow ('648) in view of Huang ('423) as applied to claims 11 and 26 respectively above, and further in view of Wang ('269).

Chow differs in failing to teach the inorganic dielectric layer comprises one of the following: CORAL, BLACK DIAMOND, FSG, carbon-doped FSG, nitrogen doped FSG, Z3MS, XLX, and HSQ.

Wang teaches, "An oxide layer **16** is formed over the metal layer 12. Although typically silicon dioxide, oxide layer **16** may include any suitable dielectric oxide material or materials, including silicon dioxide, fluorine doped silicon glass (FSG), tetraethylorthosilicate (TEOS), phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), any suitable spin-on glass, or low k polymer materials (column 4, lines 16-22).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Huang by replacing quartz (silicon dioxide) with FSG as taught Wang since both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner can normally be reached on Second Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-972-9310 for regular communications and 703-972-9311 for After Final communications.

ltue
August 8, 2002

JEFFRIE R. LUND
PRIMARY EXAMINER